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PTO/SB/05 (4/98)
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No.	AGLE0008
First Inventor or Application Identifier	Calderone et al.
Title	N-Way Demultiplexer
Express Mail Label No.	EL540885927US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

1. [X] * Fee Transmittal Form *(e.g., PTO/SB/17)* *(Submit an original and a duplicate for fee processing)*
2. [X] Specification [Total Pages 21] *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 U.S.C. 113)* [Total Sheets 5]
4. Oath or Declaration [Total Pages 2]
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 C.F.R. § 1.63(d)) *(for continuation/divisional with Box 16 completed)*
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

** NOTE FOR ITEMS 1 & 13: IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).*

5. [ ] Microfiche Computer Program *(Appendix)*
6. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. [X] Assignment Papers (cover sheet & document(s))
8. [X] 37 C.F.R.§3.73(b) Statement *(when there is an assignee)* [X] Power of Attorney
9. [ ] English Translation Document *(if applicable)*
10. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
11. [ ] Preliminary Amendment
12. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
13. [X] * Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application, Status still proper and desired
14. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
15. [ ] Other: .....

16. **If a CONTINUING APPLICATION,** *check appropriate box, and supply the requisite information below and in a preliminary amendment*

[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No _____/_____

Prior application information: Examiner _____ *Group / Art Unit:* _____

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

[X] *Customer Number or Bar Code Label* 22862 *(Insert Customer No. or Attach bar code label here)* or [ ] *Correspondence address below*

Name					
Address					
City		State		Zip Code	
Country		Telephone		Fax	

Name (Print/Type)	Michael A. Glenn	Registration No. (Attorney/Agent)	30,176
Signature		Date	9/14/2000

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JC490 U.S. PTO 09/14/00

JC511 U.S. PTO 09/661486 09/14/00

09661486 - 091400

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FEE TRANSMITTAL for FY 1999

Patent fees are subject to annual revision.
Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid. See Forms PTO/SB/09-12. See 37 C.F.R. §§ 1.27 and 1.28.

TOTAL AMOUNT OF PAYMENT ($) 688.00

Complete if Known	
Application Number	Unassigned
Filing Date	Herewith
First Named Inventor	Calderone et al.
Examiner Name	Unassigned
Group / Art Unit	Unassigned
Attorney Docket No.	AGLE0008

METHOD OF PAYMENT (check one)

1. [X] The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Deposit Account Number: 07-1445

Deposit Account Name: Michael Glenn

[X] Charge Any Additional Fee Required Under 37 CFR §§ 1.16 and 1.17

2. [ ] **Payment Enclosed:** [ ] Check [ ] Money Order [ ] Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	760	201	380	Utility filing fee	345.00
106	310	206	155	Design filing fee	
107	480	207	240	Plant filing fee	
108	760	208	380	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 345.00

2. EXTRA CLAIM FEES

	Extra Claims			Fee from below	Fee Paid
Total Claims	32	-20** =	12	X 9	= 108.00
Independent Claims	8	- 3** =	5	X 39	= 195.00
Multiple Dependent					=

**or number previously paid, if greater, For Reissues, see below

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	78	202	39	Independent claims in excess of 3
104	260	204	130	Multiple dependent claim, if not paid
109	78	209	39	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 303.00

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	380	216	190	Extension for reply within second month	
117	870	217	435	Extension for reply within third month	
118	1,360	218	680	Extension for reply within fourth month	
128	1,850	228	925	Extension for reply within fifth month	
119	300	219	150	Notice of Appeal	
120	300	220	150	Filing a brief in support of an appeal	
121	260	221	130	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,210	241	605	Petition to revive - unintentional	
142	1,210	242	605	Utility issue fee (or reissue)	
143	430	243	215	Design issue fee	
144	580	244	290	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	40.00
146	760	246	380	Filing a submission after final rejection (37 CFR § 1.129(a))	
149	760	249	380	For each additional invention to be examined (37 CFR § 1.129(b))	

Other fee (specify) _____

Other fee (specify) _____

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 40.00

SUBMITTED BY

Complete *(if applicable)*

Name (Print/Type)	Michael Glenn	*Registration No. (Attorney/Agent)*	30,176	*Telephone*	650-474-8400
Signature				*Date*	9/14/2000

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PTO/SB/10 (1-99)
Approved for use through 09/30/2000. OMB 0651-0031
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

STATEMENT CLAIMING SMALL ENTITY STATUS (37 CFR 1.9(f) & 1.27(c))--SMALL BUSINESS CONCERN

Docket Number (Optional) AGLE0008

Applicant, Patentee, or Identifier: Calderone et al.
Application or Patent No.: Unassigned
Filed or Issued: Herewith
Title: N-Way Demultiplexer

I hereby state that I am
☐ the owner of the small business concern identified below:
☒ an official of the small business concern empowered to act on behalf of the concern identified below:

NAME OF SMALL BUSINESS CONCERN AgileTV Corporation

ADDRESS OF SMALL BUSINESS CONCERN 333 Ravenswood Avenue, Bldg. 202
Menlo Park, CA 94025

I hereby state that the above identified small business concern qualifies as a small business concern as defined in 13 CFR Part 121 for purposes of paying reduced fees to the United States Patent and Trademark Office. Questions related to size standards for a small business concern may be directed to: Small Business Administration, Size Standards Staff 409 Third Street, SW, Washington, DC 20416.

I hereby state that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention described in:

☒ the specification filed herewith with title as listed above.
☐ the application identified above.
☐ the patent identified above.

If the rights held by the above identified small business concern are not exclusive, each individual, concern, or organization having rights in the invention must file separate statements as to their status as small entities, and no rights to the invention are held by any person, other than the inventor, who would not qualify as an independent inventor under 37 CFR 1.9(c) if that person made the invention, or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d), or a nonprofit organization under 37 CFR 1.9(e).

Each person, concern, or organization having any rights in the invention is listed below:
☐ no such person, concern, or organization exists.
☒ each such person, concern, or organization is listed below.

Separate statements are required from each named person, concern or organization having rights to the invention stating their status as small entities. (37 CFR 1.27)

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

NAME OF PERSON SIGNING James E. Jervis

TITLE OF PERSON IF OTHER THAN OWNER Vice President of Intellectual Property

ADDRESS OF PERSON SIGNING 333 Ravenswood Ave. Menlo Park, CA 94025

SIGNATURE James E. Jervis DATE Sept 13, 2000

N-Way Demultiplexer

BACKGROUND OF THE INVENTION

TECHNICAL FIELD

The invention relates to data transfer within a communications system, such as a digital television distribution network. More particularly, the invention relates to a technique for mediating data exchange rates among various components of a digital television distribution network by use of a novel n-way demultiplexer.

DESCRIPTION OF THE PRIOR ART

Agile TV of Menlo Park, California has developed a system that uses an extremely powerful compute engine to perform various tasks, including speech recognition and Web browsing (see System And Method Of A Multi-Dimensional Plex Communication Network, U.S. Patent Application Serial No. , filed). Due to the very high computational capabilities of the compute engine, as well as its interconnected bandwidth, a single output processor is capable of outputting a continuous data stream on the order of 2.6 gigabits per second on a single output port. The preferred compute engine may be configured with anywhere from one to sixteen output ports, although a presently preferred configuration includes two output ports.

To place the figure of 2.6 gigabits per second in perspective, this represents 96 standard 6-MHz bandwidth video channels, which is equivalent to 750 to 1000 digital television channels depending on the type of modulation used.

A key challenge created by this large volume of data is to slow the data down to interface the compute engine to a variety of traditional cable head-end

equipment, most of which operates at a much lower data rate. Further, the variance in cable television head-end configurations requires a great deal of flexibility in the number of video streams supported per interface.

It would be advantageous to provide a high performance, low cost method of distributing such high data rate output data to a number of different ports.

SUMMARY OF THE INVENTION

The invention provides a high performance, low cost method of distributing such high data rate output data to a number of different ports. Cable systems vary dramatically in the number of channels that they have to support. The invention provides a system that has the ability to have anywhere from one up to 96 different channels of output, while freely intermixing the number of channels that are bonded together under this output. For example, there can be one output having thirteen channels, another output having seven channels, another output having three channels, and another output having fifteen channels, and so on. The invention allows one to select the number of channels to be bonded together onto the output arbitrarily. This is useful in various applications that require different bandwidths. For example, in different architectures where the distribution of the signal varies, depending on the architecture of the specific cable headend.

An output clock synchronizes an output CPU with an n-way demultiplexer to allow the demultiplexer to know which output is which. To do so, the invention provides a synchronization scheme in which a synchronization string is always written to channel zero before the output is allowed to be clocked. Once

synchronization is established, each channel has its own word-length output buffer. Thus, each time the clock sends out a signal, a new word is put into the output buffer, unless it happens to be for channel zero which does not need a memory.

An address counter controls the output buffer. When the address counter is counting it is pointing to one of 95 sixteen-bit shift registers that are associated with the output buffers. For example, channel one is written with a first word, then channel two, then channel three, then channel four, and then channel five – up to channel 95. When the counter wraps around to zero, the synchronization string is expected. The address counter continues to point at zero until the synchronization string is detected. Thus, the invention provides a mechanism that automatically re-synchronizes itself. For example, in the event that something goes wrong and synchronization is lost, the invention provides a mechanism that waits for a synchronization string and that then re-synchronizes on its own.

While the data are written to the shift register, the output clock is performing a shift register function. Thus, the data are input in parallel and then shifted out in serial. On the first clock edge the zero bit is shifted out, on the next clock edge the one bit is shifted out – up through fifteen. By the time the shift register reaches fifteen and it is time to output the next bit, the system has already written the next word to that set output. Thus, there are 95 television channels in digital form that are output from the shift registers.

In some cases it is desirable to have two or more channels on a single output. The invention uses the fact that there is storage for other channels next to a preceding channel. For example, consider an output 1 and an output 2, where data are stored into two shift registers. In the invention, the two shift registers are connected together, such that by the time the system finishes outputting the first word from output 1, it automatically starts outputting the word from output 2. This is accomplished by running a clock on output 1 and output 2 at twice the rate that the clock would normally run for just output 1. In this way, the system provides throughput for two channels while synchronization is maintained within the system. Any number of channels may be bonded using this technique.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is block schematic diagram of the output section of a communications system according to the invention;

Fig. 2 is a block schematic diagram which provides an expanded view of the internal structure of an n-way demultiplexer according to the invention;

Fig. 3 is a detailed block schematic diagram of the n-way demultiplexer of Fig. 2 showing a first preferred clock selection logic circuit according to the invention;

Fig. 4 is a detailed block schematic diagram of the n-way demultiplexer of Fig. 2 showing an alternative, equally preferred clock selection logic circuit according to the invention; and

Fig. 5 is a flow diagram showing an example of a preferred synchronization sequence according to the invention.

DETAILED DESCRIPTION OF THE INVENTION

The invention provides a high performance, low cost method of distributing high data rate output data to a number of different ports.

Fig. 1 is block schematic diagram of the output section of a communications system according to the invention. In Fig. 1, an output CPU 11 is connected to a compute engine 12, 13 by a bridge circuit 15. Such circuits are very well known in the art. The system may comprise one or more CPU's.

This high speed bus provides 800 megabytes per second of bandwidth, thereby enabling sufficient connectivity to saturate the output port. It will be appreciated by those skilled in the art that other interconnect strategies may be used to implement the invention and that the implementation discussed herein is provided for purposes of example and not by way of limitation of the invention.

As shown in Fig. 1, the presently preferred output CPU actually contains two processor cores in a single package, although the method described herein is also relevant to single CPU systems. The output CPU contains a high speed, bi-directional 16-bit FIFO interface 16 which can be clocked at up to 160 MHz. At this data rate, the output CPU provides a full 2.6 gigabits of data per second to an n-way demultiplexer 18. It will be appreciated by those skilled in the art that, although the invention herein is described in connection with a specific output CPU, the invention is readily applied to other output devices.

Fig. 2 is a block schematic diagram which provides an expanded view of the internal structure of an n-way demultiplexer 18 according to the invention. In overview, the major functional blocks of the demultiplexer include:

- An output clock generator 35 which is fed to the output CPU's FIFO interface. The clock is used to transfer each word from the output CPU to the demultiplexer's inputs.

- An address counter 23 that targets an output buffer associated with each output channel. In the preferred embodiment of the invention, 96 different output buffers are available.

- Write logic that enables the current input word to be stored into the contents of the addressed output buffer.

- Shift registers 25 connected to each output buffer that provide for the serial transmission of the stored word to the associated output pin. Each of the shift registers, *e.g.* 30, 31, 32, has a carry output which is connected to the carry input of the shift register in the next lower numbered output channel.

- Clock generation logic 36 that provides for the generation of a variety of different output clocks. Eight different clocks are provided in the preferred embodiment of the invention. Each of these eight clocks may be programmed to be an integral divisor of a reference clock 34. The reference

clock may be either identical to the output clock 35 provided to the output CPU's FIFO, or it may be an integer multiple of that clock. If the reference clock is run at the CPU's output clock rate, the clock divisors may range from 1-96, enabling from one (with a divisor of 96) to 96 (with a divisor of one) output channels. If the reference clock is run at an integer multiple of the output clock associated with the output CPU, then the divisor ranges must support the same range mentioned above, multiplied by the degree b which the speed increase of the reference clock is greater than the output CPU's FIFO clock. For example, the reference clock could be run as high as sixteen times the CPU's output clock. In this case, the clock divisor ratios must range from 1 to 96 * 16.

- Clock selection logic associated with each individual output stage, which enables each output to be run at one of the eight different clock rates, independently of the other outputs. Figs. 3 and 4 provide more detailed block schematic diagrams showing alternative clock selection logic according to the invention.

In the preferred embodiment of the invention, channel 0 is reserved for the detection of synchronization information. Synchronization is necessary to ensure that the next word transferred between the output CPU and the n-way demultiplexer is written to the proper output buffer. Because the FIFO output does not contain address information it is necessary to synchronize the implicit

address associated with the output CPU's data with the address counter in the demultiplexer. Thus, the address counter is inhibited from advancing past address 0 until channel 0 is written with a synchronization string having a value of 0FFFFH via hardwired logic 50. It will be appreciated by those skilled in the art that any other synchronization string may be provided as desired.

The following is an example of a preferred synchronization sequence (see Fig. 5):

- The output CPU initially creates a data stream consisting of 95 words of 0, and sends this data through the FIFO interface (100). This ensures that the address counter in the demultiplexer is reset, regardless of its initial condition.

- Following the initial string of 0s, the output CPU writes a stream of multiplexed channel information with one word per channel (110). Channel 0 is always written with 0FFFFH, which is a string that is used to initiate synchronization (120). It will be appreciated by those skilled in the art that the initialization string is a matter of choice and need not be 0FFFFH.

- During normal operation, the output CPU interleaves data from all 95 of the current output channels together, with one word per channel (130). Prior to issuing these data to the FIFO, the CPU always writes a value of 0FFFFH initially (120), thereby maintaining synchronization. This pattern repeats indefinitely.

- If at any time channel 0 is written with any value other than 0FFFFH (140), the address counter continues to hold at 0 (150). Only after the address counter is written with 0FFFFH is the count permitted to advance to the active output channel and data are output (160).

- In the event that loss of synchronization occurs (150), FIFO data are repeatedly written to channel 0 until a value of 0FFFFH appears in the stream 120). Note that this does not inherently guarantee immediate synchronization, but it takes no more than a few loops through the counter outputs before synchronization occurs, typically within a matter of milliseconds.

In addition to the synchronization scheme discussed above, the n-way demultiplexer provides another important capability, *i.e.* the demultiplexer may be configured to support anywhere from one to 95 channels on its serial outputs in a manner which is substantially transparent to system software. Each cable system may require a different number of channels to be multiplexed onto each serial output stream. The n-way demultiplexer enables the number of channels that are bonded together to be set independently for each output channel.

To accomplish this task, at system initialization each output channel is configured to run at an appropriate clock rate. To bond channels together, it is only necessary to select the same rate for sequential output channels, and then the

lowest numbered channel's output is actually used for output, while the remaining output pins are ignored. For example, if it is necessary to bond eight outputs together into a serial data stream, inputs 10-18 could all be programmed with a clock divisor (96/8=12), meaning that they are clocked at a rate which is $1/12^{th}$ that of the CPU's FIFO clock.

Once data are written to these outputs as described above, the data that have been written begin serially clocking out to the output pin. In the case of channel 10, the first sixteen clocks produce the data for channel 10, as expected. However, continued clocking then produces the output data for channel 11, then channel 12, and so on. This occurs due to the carry-in carry-out connections described above (see buffers 30, 31, 32 on Fig. 2). Note that it is not necessary to change anything other than the output clock selection when bonding channels. Even though the carry input of the highest numbered channel in the group is still connected to a different output group, the data shifted in are never propagated onto the output pin, so it may be safely ignored.

Due to the interdependence between output groups, any number of channels may be bonded together in any number of groups. This provides superior flexibility in a broad variety of environments and at very low cost.

Although the invention is described herein with reference to the preferred embodiment, one skilled in the art will readily appreciate that other applications may be substituted for those set forth herein without departing from the spirit and scope of the present invention. Accordingly, the invention should only be limited by the Claims included below.

CLAIMS

1. A method for distributing high data rate output data to a number of different ports, comprising the steps of:

providing an output module having a plurality of different output channels;

providing a demultiplexer in communication with said output module for receiving said output channels; and

providing an output clock for synchronizing said output module with said demultiplexer.

2. The method of Claim 1, further comprising the step of:

bonding together any predetermined number of channels for each of said ports independently of each of said other ports.

3. The method of Claim 1, further comprising the step of:

providing a synchronization scheme in which a synchronization string is always written to a particular channel before said output channels are allowed to be clocked.

4. The method of Claim 3, further comprising the step of:

providing each output channel with its own output buffer;

wherein, once synchronization is established, each time said clock sends out a signal, a new word is put into an appropriate output buffer.

5. The method of Claim 4, further comprising the step of:

providing an address counter for controlling each said output buffer;

wherein said address counter waits for said synchronization string before counting through each of said output buffers.

6. The method of Claim 5, further comprising the step of:

providing a shift register associated with each said output buffer for receiving data in parallel as an input and for outputting said data in a serial fashion to an associated output buffer.

7. The method of Claim 6, further comprising the steps of:

connecting said shift registers together, such that by the time a first word is output from a first output buffer a next word may begin being output from said first output buffer; and

running a clock on said first output buffer and said next output buffer at a multiple of a rate that said clock would normally run for just said first output buffer.

8. A demultiplexer, comprising:

an output clock generator for transferring data from an output module to a demultiplexer input;

an address counter associated with said demultiplexer for targeting an output buffer associated with each of a plurality of output channels;

write logic associated with said demultiplexer for enabling current input data to be stored into an addressed output buffer;

a plurality of shift registers associated with said demultiplexer, one each connected to each output buffer for providing serial transmission of said stored data to an associated output.

9. The demultiplexer of Claim 8, wherein each of said shift registers has a carry output which is connected to a carry input of a shift register in a next lower numbered output channel.

10. The demultiplexer of Claim 9, further comprising:

clock generation logic for generating a plurality of different output clocks;

wherein each of said output clocks may be programmed to be an integral divisor of a reference clock;

wherein said reference clock may be either identical to an output clock provided to said output module, or it may be an integer multiple of said clock.

11. The demultiplexer of Claim 10, further comprising:

clock selection logic associated with each individual output buffer for enabling each output buffer to be run at one of a plurality of different clock rates, independently of said other output buffers.

12. The demultiplexer of Claim 8, wherein a channel is reserved for detection of synchronization information to ensure that data transferred between said output module and said demultiplexer is written to a proper output buffer.

13. The demultiplexer of Claim 12, wherein said address counter is inhibited from advancing past a first address until said reserved channel is written with a synchronization string.

14. A synchronization method for a demultiplexer, comprising the steps of:

initially creating a data stream with an output module to reset an address counter in said demultiplexer regardless of said demultiplexer's initial condition;

said output module writing a stream of multiplexed channel information with one word per channel, wherein a reserved channel is always written with a string that is used to initiate synchronization;

said output module interleaving data from all current output channels together, with one word per channel, wherein said output module always writes said string prior to issuing said data; and

providing an address counter that continues to hold at said reserved channel if at any time said reserved channel is written with any value other than said string, wherein a count is permitted to advance to an active output channel and data are output only after said address counter is written with said string.

15. The synchronization method of Claim 14, wherein data are repeatedly written to said reserved channel by said output module until said string appears in said data stream in the event that a loss of synchronization occurs.

16. A method for multiplexing a different number of channels onto each of a plurality of serial output streams, comprising:

providing a demultiplexer for enabling a number of channels that are bonded together to be set independently for each output channel;

said demultiplexer:

at system initialization, configuring each output channel to run at an appropriate clock rate;

selecting a same rate for sequential output channels; and

using a lowest numbered channel's output for actual data output, while ignoring remaining outputs.

17. An apparatus for distributing high data rate output data to a number of different ports in a system having an output module having a plurality of different output channels, said apparatus comprising:

a demultiplexer in communication with said output module for receiving said output channels; and

an output clock for synchronizing said output module with said demultiplexer.

18. The apparatus of Claim 17, further comprising:

means for bonding together any predetermined number of channels for each of said ports independently of each of said other ports.

19. The apparatus of Claim 17, further comprising:

a synchronization scheme in which a synchronization string is always written to a particular channel before said output channels are allowed to be clocked.

20. The apparatus of Claim 19, further comprising:

an output buffer each output channel;

wherein, once synchronization is established, each time said clock sends out a signal, a new word is put into an appropriate output buffer.

21. The apparatus of Claim 20, further comprising:

an address counter for controlling each said output buffer;

wherein said address counter waits for said synchronization string before counting through each of said output buffers.

22. The apparatus of Claim 21, further comprising:

a shift register associated with each said output buffer for receiving data in parallel as an input and for outputting said data in a serial fashion to an associated output buffer.

23. The apparatus of Claim 22, wherein said shift registers are connected together, such that by the time a first word is output from a first output a next word may begin being output from said first output; and further comprising:

a clock for clocking said first output and said next output, said clock running at a multiple of a rate that said clock would normally run for just said first output.

24. A method for demultiplexing, comprising the steps of:

transferring data from an output module to a demultiplexer input with an output clock generator;

targeting an output buffer associated with each of a plurality of output channels with an address counter associated with said demultiplexer;

enabling current input data to be stored into an addressed output buffer with write logic associated with said demultiplexer;

providing serial transmission of said stored data to an associated output with a plurality of shift registers associated with said demultiplexer, one each connected to each output buffer.

25. The method of Claim 24, wherein each of said shift registers has a carry output which is connected to a carry input of a shift register in a next lower numbered output channel.

26. The method of Claim 25, further comprising the step of:

generating a plurality of different output clocks with clock generation logic;

wherein each of said output clocks may be programmed to be an integral divisor of a reference clock;

wherein said reference clock may be either identical to an output clock provided to said output module, or it may be an integer multiple of said clock.

27. The method of Claim 26, further comprising the step of:

enabling each output buffer to be run at one of a plurality of different clock rates, independently of said other output buffers with clock selection logic associated with each individual output buffer.

28. The method of Claim 24, wherein a channel is reserved for detection of synchronization information to ensure that data transferred between said output module and said demultiplexer is written to a proper output buffer.

29. The method of Claim 28, wherein said address counter is inhibited from advancing past a first address until said reserved channel is written with a synchronization string.

30. A synchronization apparatus for a demultiplexer, comprising:

an output module for initially creating a data stream to reset an address counter in said demultiplexer regardless of said demultiplexer's initial condition;

said output module writing a stream of multiplexed channel information with one word per channel, wherein a reserved channel is always written with a string that is used to initiate synchronization;

said output module interleaving data from all current output channels together, with one word per channel, wherein said output module always writes said string prior to issuing said data; and

an address counter that continues to hold at said reserved channel if at any time said reserved channel is written with any value other than said string,

wherein a count is permitted to advance to an active output channel and data are output only after said address counter is written with said string.

31. The synchronization apparatus of Claim 30, wherein data are repeatedly written to said reserved channel by said output module until said string appears in said data stream in the event that a loss of synchronization occurs.

32. An apparatus for multiplexing a different number of channels onto each of a plurality of serial output streams, comprising:

a demultiplexer for enabling a number of channels that are bonded together to be set independently for each output channel;

said demultiplexer comprising:

means for configuring each output channel to run at an appropriate clock rate at system initialization;

means for selecting a same rate for sequential output channels; and

means for using a lowest numbered channel's output for actual data output, while ignoring remaining outputs.

N-Way Demultiplexer

ABSTRACT

Cable systems vary dramatically in the number of channels that they have to support. The invention provides the ability to have anywhere from one up to 96 different channels of output, while freely intermixing the number of channels that are bonded together under this output. The invention allows one to select the number of channels to be bonded together onto the output arbitrarily. In the preferred embodiment of the invention, an output clock synchronizes an output CPU with an n-way demultiplexer to allow the demultiplexer to know which output is which. To do so, the invention provides a synchronization scheme in which a synchronization string is always written to channel zero before the output is allowed to be clocked. Once synchronization is established, each channel has its own word-length output buffer. Thus, each time the clock sends out a signal, a new word is put into the output buffer, unless it happens to be for channel zero which does not need a memory. An address counter controls the output buffer. When the address counter is counting it is pointing to one of the 95 by sixteen shift registers that are in the output buffers. For example, channel one is written with a first word, then channel two, then channel three, then channel four, and then channel five – up to channel 95. When the counter wraps around to zero, the synchronization string is expected. The address counter continues to point at

zero until the synchronization string is detected. Thus, the invention automatically re-synchronizes. While the data are written to the shift register, the output clock is performing a shift register function. Thus, the data are input in parallel and then shifted out in serial. On the first clock edge the zero bit is shifted out, on the next clock edge the one bit is shifted out – up through fifteen for each sixteen-bit shift register. By the time the shift register reaches fifteen and it is time to output the next bit, the system has already written the next word to that set output. Thus, there are 95 television channels in digital form that are output from the shift registers. In some cases it is desirable to have two or more channels on a single output. The invention uses the fact that there is storage for other channels next to a preceding channel. For example, consider an output 1 and an output 2, where data are stored into two shift registers. In the invention, the two shift registers are connected together, such that by the time the system finishes outputting the first word from output 1, it automatically starts outputting the word from output 2. This is accomplished by running a clock on output 1 and output 2 at twice the rate that the clock would normally run for just output 1. In this way, the system provides throughput for two channels while system synchronization is maintained within the system. Any number of channels may be bonded using this technique.

FIGURE 1

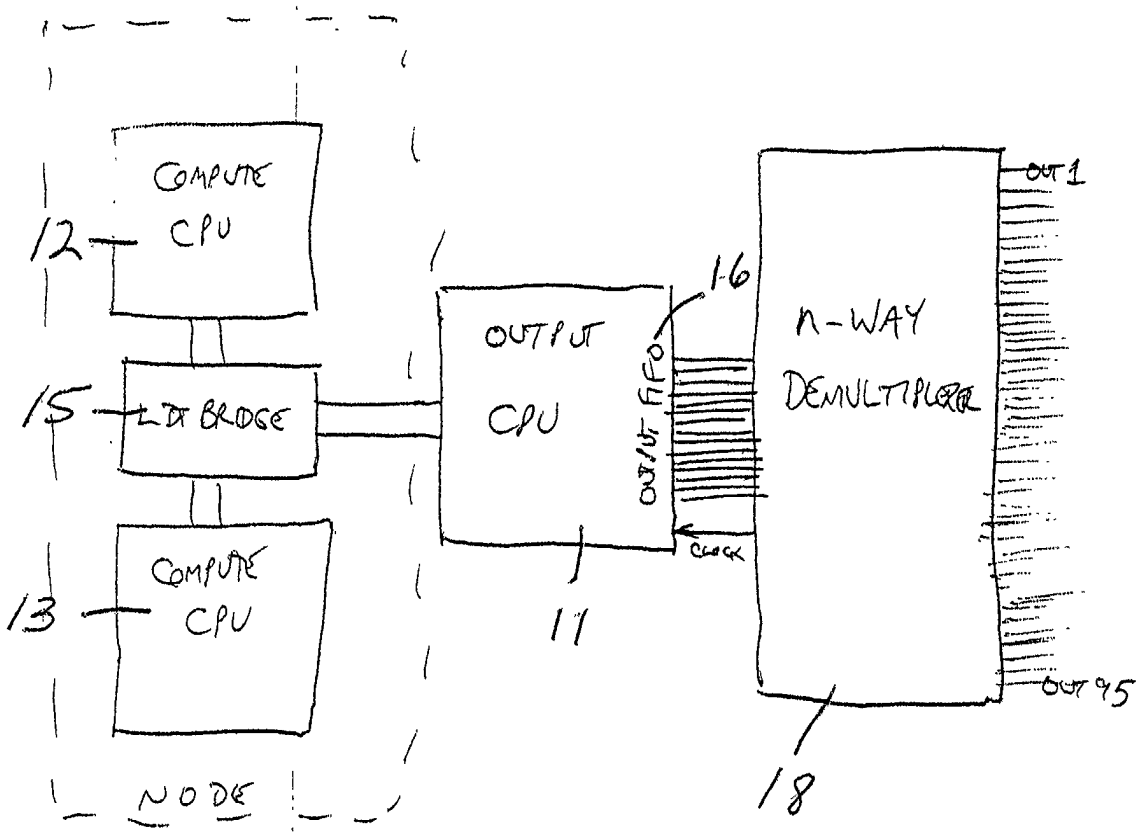


FIGURE 2

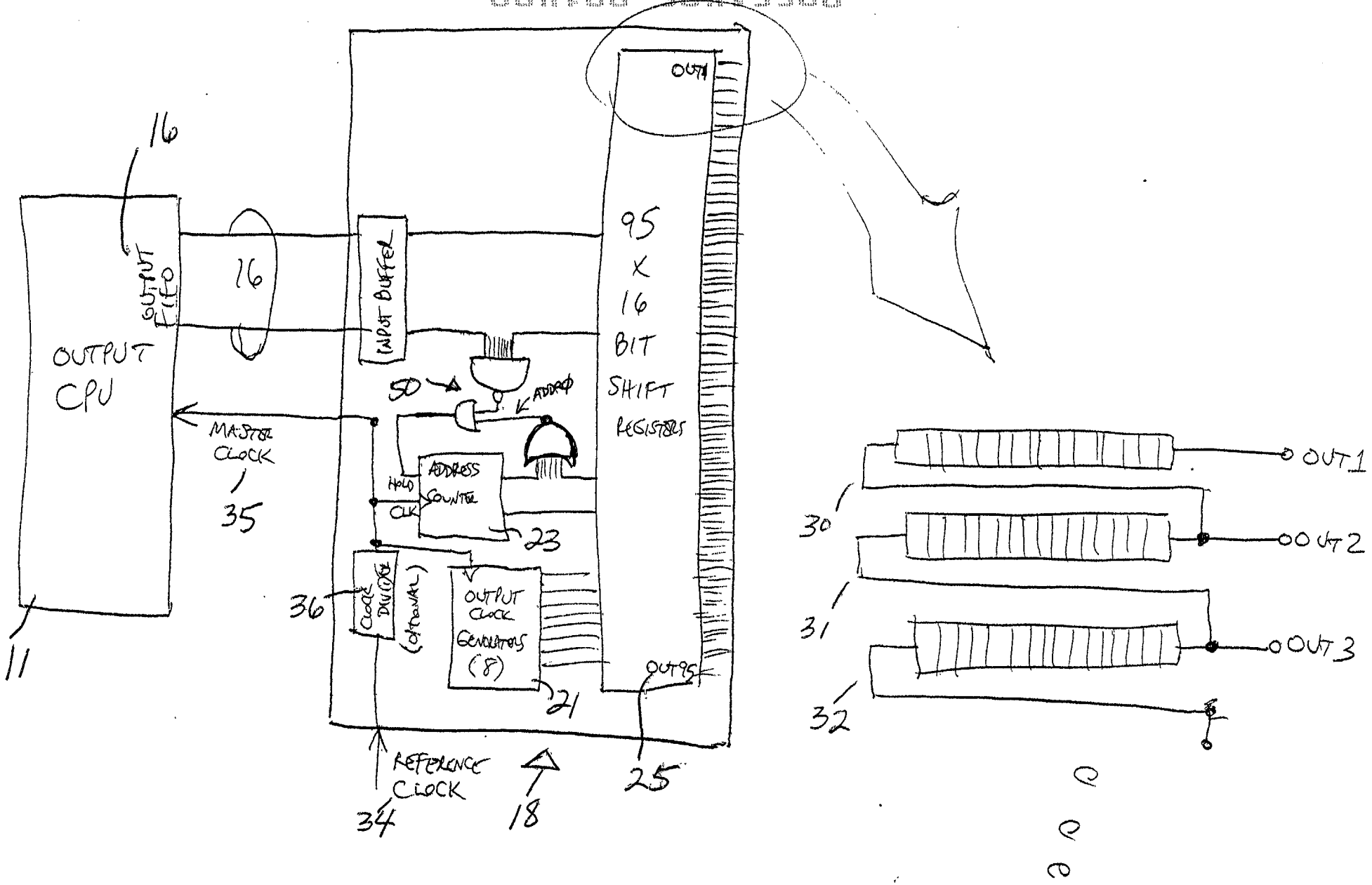
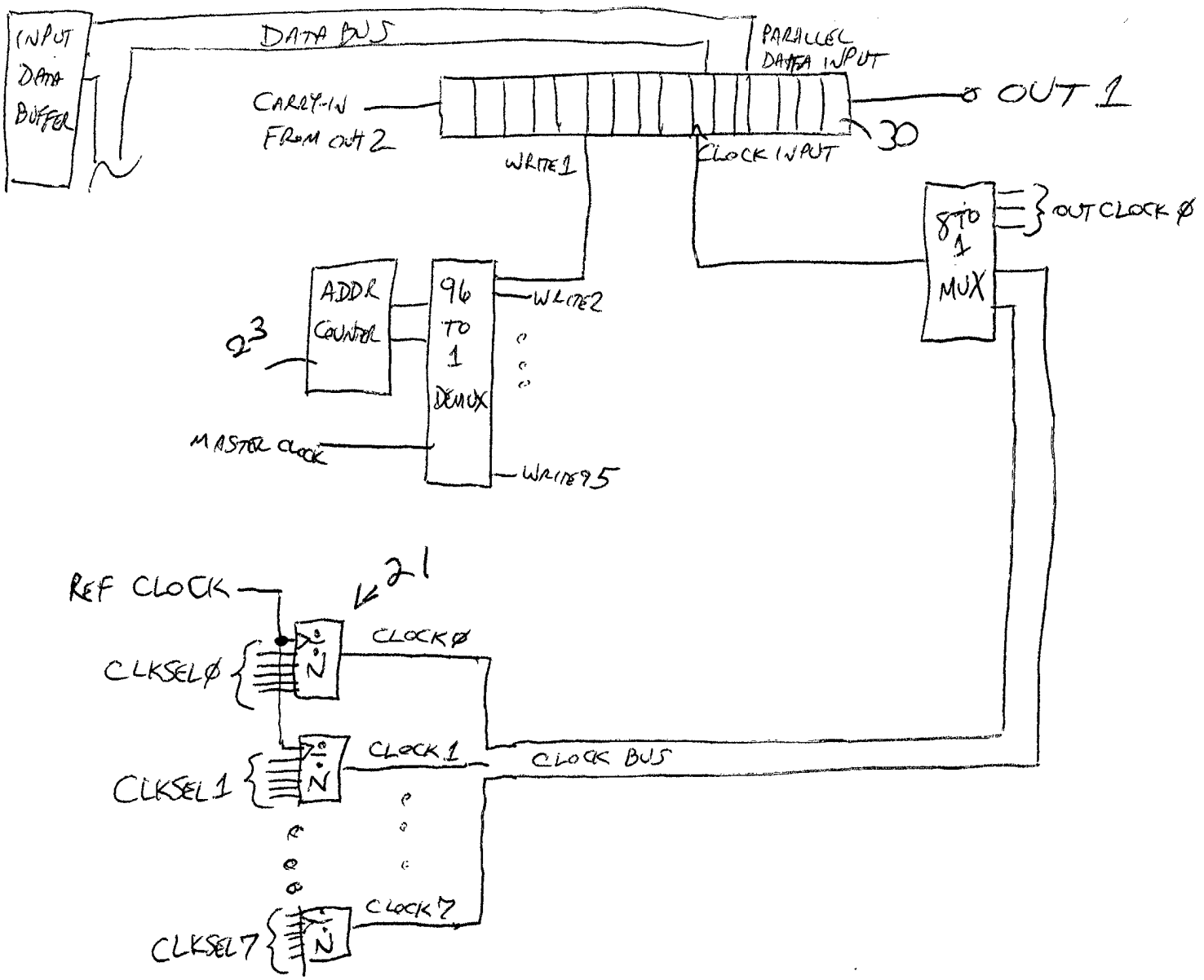
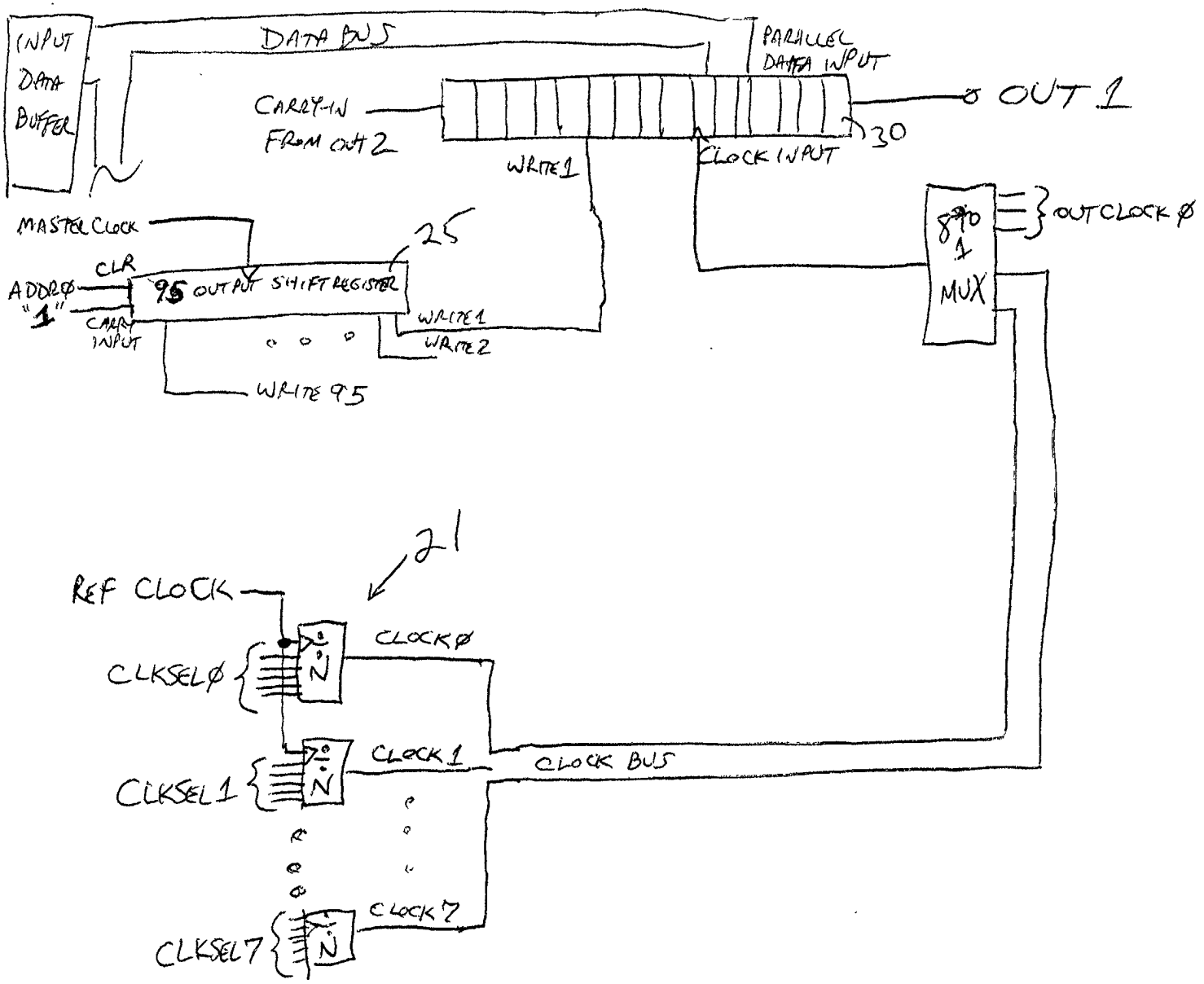

16
OUTPUT FIFO
16
OUTPUT CPU
11
INPUT BUFFER
95 X 16 BIT SHIFT REGISTERS
OUT1
50
ADDR0
MASTER CLOCK
35
HOLD
CLK
ADDRESS COUNTER
23
36
CLOCK DIVIDER (OPTIONAL)
OUTPUT CLOCK GENERATORS (8)
21
OUT95
25
REFERENCE CLOCK
34
18
30
31
32
OUT 1
OUT 2
OUT 3

FIG 9


INPUT DATA BUFFER
DATA BUS
PARALLEL DATA INPUT
CARRY-IN FROM OUT 2
OUT 1
30
WRITE 1
CLOCK INPUT
8 TO 1 MUX
OUT CLOCK Ø
ADDR COUNTER
2^3
96 TO 1 DEMUX
WRITE 2
WRITE 95
MASTER CLOCK
21
REF CLOCK
CLKSEL Ø
CLOCK Ø
CLKSEL 1
CLOCK 1
CLOCK BUS
CLKSEL 7
CLOCK 7


INPUT DATA BUFFER
DATA BUS
PARALLEL DATA INPUT
CARRY-IN FROM OUT 2
OUT 1
30
WRITE 1
CLOCK INPUT
MASTER CLOCK
25
CLR
ADDR Ø
"1"
95 OUTPUT SHIFT REGISTER
CARRY INPUT
WRITE 1
WRITE 2
WRITE 95
8 TO 1 MUX
OUT CLOCK Ø
21
REF CLOCK
CLOCK Ø
CLKSEL Ø
N
CLOCK 1
CLKSEL 1
CLOCK BUS
CLOCK 7
CLKSEL 7

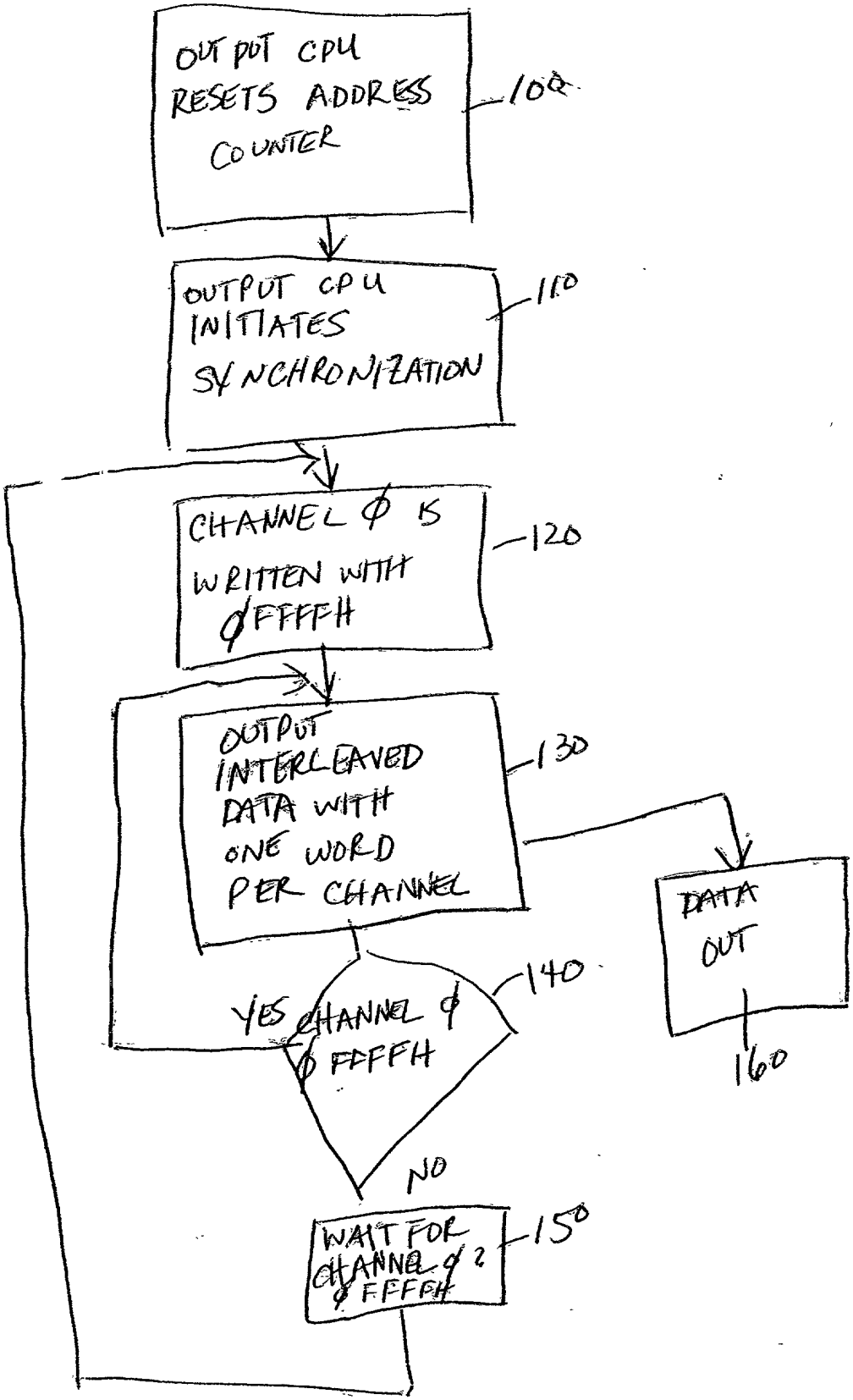


Fig. 5

Attorney Docket No. AGLE0008

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name;

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

N-WAY DEMULTIPLEXER

the specification of which (check one) X is attached hereto, or ___ was filed on _____ as Application Serial No. _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

==========

I hereby claim foreign priority benefits under Title 35, United Sates Code, Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
			Yes	No
_____			___	___
Number	Country	Day/Month/Year Filed		
_____			___	___
Number	Country	Day/Month/Year Filed		

==========

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith:

MICHAEL A. GLENN, Reg. No. 30,176
DONALD M. HENDRICKS, Reg. No. 40,355
CHRISTOPHER PEIL, Reg. No. 45,005
EARLE JENNINGS, Reg. No. 44,804

Attorney Docket No. AGLE0008

JACK J'MAEV, Reg. No. 45,669

SEND CORRESPONDANCE TO:

MICHAEL A. GLENN 3475 Edison Way, Suite L, Menlo Park, CA 94025

==========

I hereby claim the benefit under Title 35, United States code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application Ser. No.	Filing Date	Status: Patented, Pending, Abandoned

==========

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor: THEODORE CALDERONE

Inventor's signature _____ Date _____

Residence 422 Portofino Drive, #3, San Carlos, California 94070

Post Office Address Same

Citizenship United States of America

Full name second inventor: MARK J. FOSTER

Inventor's signature _____ Date _____

Residence 4157 Interdale Way, Palo Alto, California 94306

Post Office Address Same

Citizenship United States of America